REMARKS

The application has been reviewed in light of the Office Action dated May 30, 2003. Claims 1-39 are pending and presented for examination in this application, with claims 1, 9, 17, 25, 29, 33 and 37-39 being in independent form.

Claims 1, 9, 17, 25, 29, 33 and 37-39 have been amended hereby to place the claims in better form for examination and to clarify the claimed invention, without narrowing the scope of the claims.

Claims 25-32 were rejected under the judicially created doctrine of obviousness-type double patenting as allegedly unpatentable over claim 4 of U.S. Patent No. 6,094,527. Claims 33-36 and 39 were rejected under the judicially created doctrine of obviousness-type double patenting as purportedly unpatentable over claim 6 of U.S. Patent No. 6,094,527. Claims 1-8 were rejected under the judicially created doctrine of obviousness-type double patenting over claim 1 of U.S. Patent No. 6,094,527. Claims 17-24 were rejected under the judicially created doctrine of obviousness-type double patenting as allegedly unpatentable over claim 3 of U.S. Patent No. 6,094,527. Claims 9-16 were rejected under the judicially created doctrine of obviousness-type double patenting as allegedly unpatentable over claim 2 of U.S. Patent No. 6,094,527. Claim 38 was rejected under the judicially created doctrine of obviousness-type double patenting as allegedly unpatentable over claim 4 of U.S. Patent No. 6,094,527.

Applicants submit concurrently herewith a Terminal Disclaimer. Accordingly, Applicants respectfully request that the rejections under the judicially-created doctrine of obviousness type double-patent be withdrawn.

Claims 1-39 were rejected under 35 U.S.C. §101 as allegedly lacking utility and under 35 U.S.C. §112, first paragraph. According to the Office Action, the stored executable code as recited in the claims is not actually executed.

In response, without conceding the correctness of the Examiner's position, but solely to advance prosecution of the subject application, the claims have been amended to clarify the subject matter Applicants claim as the invention and to place the claims in better form for examination, without narrowing the scope of the claims.

Accordingly, withdrawal of the rejections under 35 U.S.C. §101 and under 35 U.S.C. §112, first paragraph is respectfully requested.

Claims 1-39 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent 5,943,487 to Messerman et al. in view of U.S. Patent No. 6,324,678 to Dangelo et al. ("Dangelo '678"), and further in view of U.S. Patent No. 5,867,397 to Koza et al., and further in view of the Microsoft Press Computer Dictionary, Third Edition. Claims 1-39 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,535,370 to Raman et al. in view of U.S. Patent No. 5,521,834 to Crafts et al. and further in view of U.S. Patent No. 5,493,508 to Dangelo et al. ("Dangelo '508").

Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit that independent claims 1, 9, 17, 25, 29, 33, and 37-39 are patentable over the cited art, for at least the following reasons.

The present application relates to estimating power consumption of an integrated circuit. As portable electronic devices proliferate through our society, an accurate estimation of power consumption by the

devices is often desired during the design and simulation stage. As discussed in the application at pages 1-2, conventional methods of estimating power consumed by integrated circuits include (1) determining, from logic simulations, the number of operation events at terminals or pins of each basic cell and estimating power consumption based on the number of events and pre-established power consumption data, or (2) estimating power consumption based on collected information for each basic cell regarding changes over time in output voltage signals, program instructions for the operation modes, and power consumption by the basic cells. The conventional methods, however, do not accurately estimate power consumption for integrated circuits.

Applicants found that power consumption by integrated circuits may be more accurately estimated by using information collected during logic simulation to estimate current consumed by mega cells and current consumed by basic cells.

For example, each of independent claims 1 and 9 relates to a computer readable medium including computer executable code stored thereon. According to claim 1, the code is executable by a processor to perform a method for estimating power consumption of an integrated circuit which includes (a) simulating logic of basic and mega cells of the integrated circuit, (b) estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells

based on the logic simulations and pre-established power consumption data, (c) estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and (d) combining the first and second values to obtain the power consumption of the integrated circuit.

According to claim 9, the code is executable by a processor to perform a method for estimating electric power consumed by basic cells and mega cells of an integrated circuit to estimate total power consumed by the integrated circuit which includes simulating logic of said basic cells and said mega cells, wherein each function of each mega cell for logic simulation is defined by hardware description language, estimating a current consumed by the basic cells for estimating a first value of electric power consumed by said basic cells based on logic simulation results from said logic simulations and pre-established power consumption data for each logic state of each input and output terminal of said basic cells, estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate said current consumed by the mega cells for estimating a second value of electric power consumed by said mega cells based on logic simulation results from said logic simulations and pre-established power consumption data for said logic states, variables in the function description, and said operating frequencies at each input and output terminal of each mega cell, and adding said first and said second values of the power consumption to

determine the total power consumption for the integrated circuit.

Messerman, as understood by Applicants, relates to extraction of a resistor network from an integrated circuit polygon layout. Operation of the resistor network is simulated to perform electromigration (which is the motion of ions through a conductor in response to the passage of current through the conductor) analysis, the results of which can then be used to estimate the reliability of the integrated circuit.

As acknowledged in the Office Action, Messerman which is cited as a primary reference does not disclose or suggest several aspects of the claimed invention.

However, the Office Action cites Messerman, column 1, line 12 through column 2, line 46, and column 7, lines 44-63, as alleged support that Messerman discloses code for estimating electric power consumed by the resistor network and pre-established power consumption data and code for determining the power consumption of the integrated circuit's resistor network. Applicants respectfully disagree.

Messerman, column 1, line 12 through column 2, line 46 discloses conventional techniques for extracting a resistor network from a symbolic layout of an integrated circuit, and using the resistor network to analyze electromigration within the circuitry of the integrated circuit. Messerman, column 7, lines 44-63, discloses a sequence of steps for identifying electromigration violations and generating a composite map of the electromigration violations.

Applicants find no teaching or suggestion in Messerman of a method for estimating electric power consumed by basic cells and mega cells of an integrated circuit to estimate total power consumed by the

integrated circuit.

Accordingly, Applicants maintain that it would not have been obvious to one of ordinary skilled in the art to make any combination of the references which includes Messerman as a starting point, without using the claimed invention as a roadmap in impermissible hindsight for piecing together the disclosures of the cited references. Furthermore, Applicants submit that one looking to devise a technique for estimating electric power consumed by basic cells and mega cells of an integrated circuit to estimate total power consumed by the integrated circuit would not have looked to the teachings of Messerman, since the reference does not purport to provide teachings in that field.

Dangelo '678, as understood by Applicants, relates to methodologies for deriving a valid structural description of a circuit or system (i.e. device) from a behavioral description thereof. Typically, a designer specifies the desired behavior of the device in a high-level language, such as VHDL. The description includes high-level timing goals. Next, starting with the VHDL behavioral description of a design, the designer iterates through simulation and design changes until the desired behavior is obtained. Next, the design is partitioned into a number of architectural blocks.

Dangelo '678, column 36, line 35 through column 41, line 52, discloses techniques for estimating power consumption in integrated circuits which includes two parts: static power consumption and dynamic power consumption. Static power dissipation is calculated by multiplying, for each logic device or gate in the circuit, a leakage current (i.e. a static current draw) of the device and a supply voltage, and summing the products for the entire collection of logic

devices in the circuit. Dynamic power dissipation for a CMOS device is calculated using output load capacitance, supply voltage, clock cycle, and the number of switching transitions per clock cycle as parameters.

However, Applicants find no teaching or suggestion in Dangelo of estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and combining the first and second values to obtain the power consumption of the integrated circuit.

Koza, as understood by Applicants, relates to automated design of complex structures (such as circuits) using genetic algorithms. The behavior of the developed structure is determined, compared to the predetermined design goals and then evolved until it meets the design goals. Simulations and fitness measures as discussed in Koza focus solely on circuit behavior in terms of inputs and outputs. Koza is cited in the Office Action as purportedly disclosing measuring alternating current of logic cells.

Microsoft Press Computer Dictionary is cited in the Office Action as disclosing use of various computer readable media.

However, Applicants find no teaching or suggestion in the cited

art of a computer readable medium including computer executable code stored thereon which is executable by a processor to perform a method for estimating power consumption of an integrated circuit which includes (a) simulating logic of basic and mega cells of the integrated circuit, (b) estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, (c) estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and (d) combining the first and second values to obtain the power consumption of the integrated circuit, as recited in independent claim 1.

Raman, as understood by Applicants, relates to current and power consumption analysis of a circuit through simulation with a model of the circuit. According to Raman, input test vectors are used to drive the model, and a simulator which operates the model maintains a toggle count for each device of the circuit. A characterization table is generated which contains an average switching current value of a type of a device for different values of capacitive loads. An activity factor can then be generated based on the number of the toggle count during a sample time period and the number of clock cycles during the sample period. Using the activity period, the current is determined

from the average switching current for the device times the activity factor. The current can then be used to perform such calculations as power consumption and electromigration testing.

The Office Action acknowledges that Raman does not disclose or suggest mega cells and calculating the alternating current component for each cell.

In addition, Applicants find no teaching or suggestion in Raman of estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data.

Crafts, as understood by Applicants, relates to techniques for approximating power dissipation of CMOS circuits. A determination is made of the capacitive load for each cell in a netlist for the CMOS circuit, from cell library data sheets, and the capacitive loads of the interconnects between stages are estimated. A switching rate for each cell is then calculated using one of two alternative methods. The first method assumes that the patterns of input signals are statistically independent, and thus estimates the switching rate from the structure of the cell and the switching rates of the inputs. The second method uses known information concerning the relative times when the input signals are high or low to determine the switching rate of the cell. Once the switching rate is known, the output frequency for the cell can be determined. The power dissipation for each cell is then calculated

by multiplying the output frequency by the capacitive load. The dynamic power dissipation for the circuit is determined by summing the power dissipation terms for each of the cells making up the netlist.

Crafts was cited in the Office Action as purportedly disclosing calculating the alternating current component for each cell.

However, Applicants find no teaching or suggestion in Crafts of estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data.

Dangelo '508, as understood by Applicants, relates to generating structural descriptions of complex digital devices from high-level descriptions and specifications.

Dangelo '508 was cited in the Office Action as purportedly disclosing mega cells and hardware description languages.

However, Applicants simply does not find teaching or suggestion in the cited art of a computer readable medium including computer executable code stored thereon which is executable by a processor to perform a method for estimating power consumption of an integrated circuit which includes estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for

estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, as recited in independent claim 1.

Accordingly, Applicants submit independent claim 1 is patentable over the cited art.

Independent claims 9, 17, 25, 29, 33, and 37-39 are believed to be patentable over the cited art for at least similar reasons.

The Office is hereby authorized to charge any additional fees that may be required in connection with this response and to credit any overpayment to our Deposit Account No. 03-3125.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Entry of this response and allowance of this application are respectfully requested.

Respectfully submitted,

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